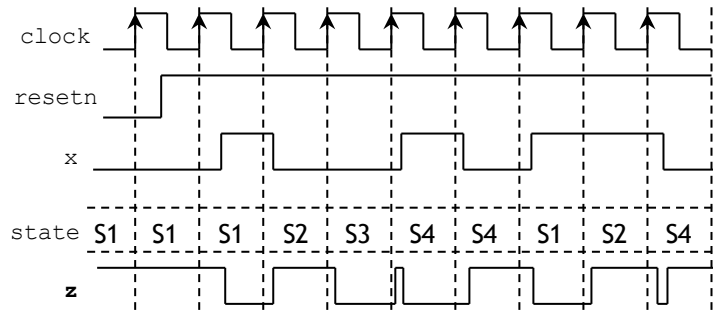
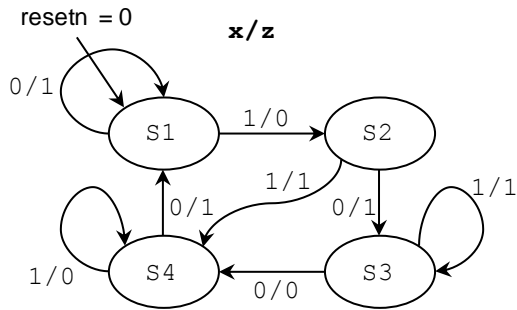


Solutions - Quiz 3 (Online Section)

(Due date: November 1st by 11:00 am)

PROBLEM 1 (20 PTS)

- Complete the timing diagram of the following state machine:



PROBLEM 2 (25PTS)

- Complete the timing diagram of the circuit whose VHDL description is shown below:

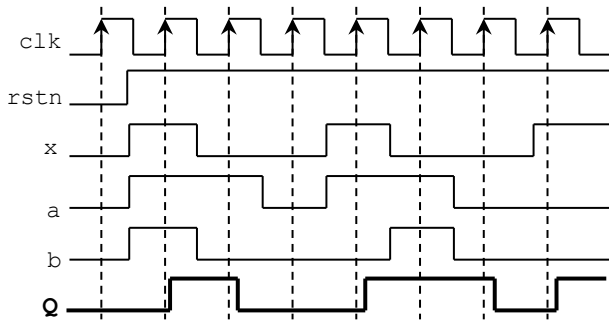
```

library ieee;
use ieee.std_logic_1164.all;

entity circ is
    port ( rstn, a,b, x, clk: in std_logic;
          q: out std_logic);
end circ;
    
```

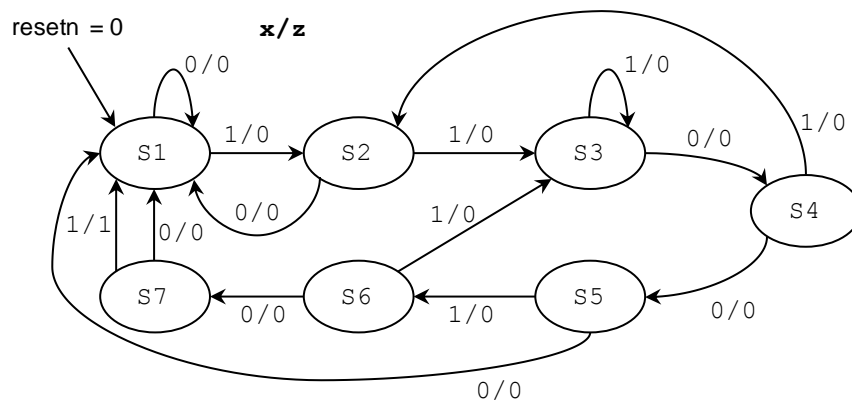
```

architecture bhv of circ is
    signal qt: std_logic;
begin
    process (rstn, clk, a, b, x)
    begin
        if rstn = '0' then
            qt <= '0';
        elsif (clk'event and clk = '1') then
            if x = '1' then
                qt <= not(qt);
            else
                qt <= a and b;
            end if;
        end if;
    end process;
    q <= qt;
end bhv;
    
```



PROBLEM 3 (25 PTS)

- Sequence detector (with overlap): Draw the state diagram of a circuit that detects the following sequence: 1100101. The detector must assert an output 'z=1' when the sequence is detected.



PROBLEM 4 (30 PTS)

- Complete the timing diagram of the following circuit. $Q = Q_4Q_3Q_2Q_1Q_0$

