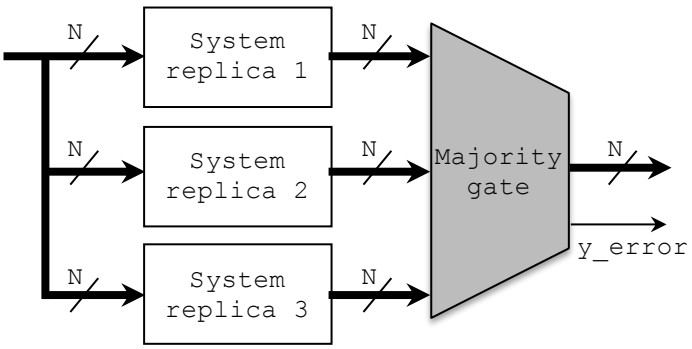
Notes - Chapter 4

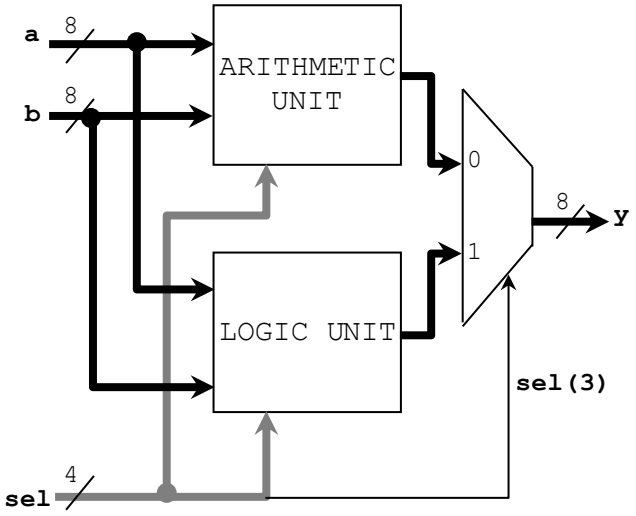
TRIPLE MODULE REDUNDANCY: MAJORITY GATE

- Three systems perform the same identical process (the input data is also identical for the three systems). The three outputs go into a majority-voting system (called 'majority gate') to produce a single output.
- If at least two systems produce identical outputs, then the majority gate will pick that output. If the three system produce different results, the majority gate will assert an error flag (`y_error = '1'`).



ARITHMETIC-LOGIC UNIT (ALU)

- This circuit carries out two types of operations: logic (or bit-wise) and arithmetic.
- In this example, the inputs `a[7..0]` and `b[7..0]` are 8-bits wide. The numbers' representation is 2's complement.

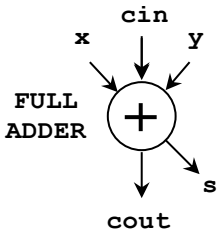


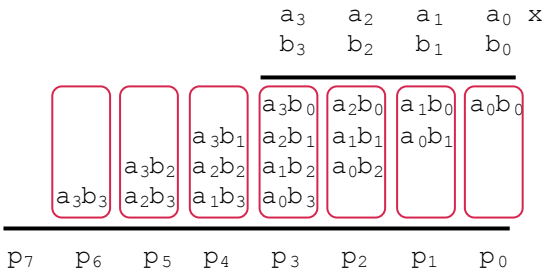
- The output is selected via the input `sel[3..0]` in the following manner:

sel	Operation	Function	Unit
0000	y <= a	Transfer 'a'	Arithmetic
0001	y <= a + 1	Increment 'a'	
0010	y <= a - 1	Decrement 'a'	
0011	y <= b	Transfer 'b'	
0100	y <= b + 1	Increment 'b'	
0101	y <= b - 1	Decrement 'b'	
0110	y <= a + b	Add 'a' and 'b'	
0111	y <= a - b	Subtract 'b' from 'a'	
1000	y <= not a	Complement 'a'	Logic
1001	y <= not b	Complement 'b'	
1010	y <= a AND b	AND	
1011	y <= a OR b	OR	
1100	y <= a NAND b	NAND	
1101	y <= a NOR b	NOR	
1110	y <= a XOR b	XOR	
1111	y <= a XNOR b	XNOR	

MULTIPLIER CIRCUIT (POSITIVE NUMBERS)

Multiplication of Positive Numbers (4-bit case):





Array Multiplier: