Solutions - Quiz 4
(December 5th @ 9:30 am)

PROBLEM 1 (40 pts)
- Complete the timing diagram of the following FSM (represented in ASM form):

```
S1
resetn=0
sclr ← 1

S2
S
1
0

S3
done ← 1

0
S
1
```

PROBLEM 2 (30 pts)
- Provide the state diagram (in ASM form) of the FSM whose VHDL description is listed below:

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port(
    clk, rstn: in std_logic;
    a, b: in std_logic;
    x, w, z: out std_logic);
end circ;

architecture behavioral of circ is
  type state is (S1, S2, S3);
  signal y: state;
begin
  Transitions: process (rstn, clk, a, b)
  begin
    if rstn = '0' then
      y <= S1;
    elsif (clk'event and clk = '1') then
      case y is
        when S1
          if a = '1' then y <= S2; else y <= S1; end if;
        when S2
          if a = '1' then y <= S2; else y <= S1; end if;
        when S3
          if b = '1' then y <= S3; else y <= S1; end if;
      end case;
    end if;
  end process;

  Outputs: process (y, a)
  begin
    x <= '0'; w <= '0'; z <= '0';
    case y is
      when S1 => if a = '1' then z <= '1'; end if;
      when S2 => x <= '1';
      when S3 => w <= '1';
    end case;
  end process;
end behavioral;
```
Problem 3 (30 pts)

- Basic Processor:
  
  **Available Registers:** R0 (register 0, 4 bits), R1 (register 1, 4 bits), PC (program counter, 4 bits), OUT (output register, 4 bits), IR (instruction register, 8 bits)

  **Instruction Memory:** Stores up to 16 8-bit instructions.

  **Instruction Set:** Instructions are specified on the Instruction Register (IR):

  \[ \begin{array}{c|c|c}
  \text{OPCODE} & \text{DR} & \text{SR} \\
  \hline
  000 & \text{MOV} & \text{DR} \leftarrow \text{SR} \\
  001 & \text{LOADI} & \text{DR} \leftarrow \text{DATA}, \text{DATA} = \text{IR}[3..0] \\
  010 & \text{ADD} & \text{DR} \leftarrow \text{DR} + \text{SR} \\
  011 & \text{ADDI} & \text{DR} \leftarrow \text{DR} + \text{DATA}, \text{DATA} = \text{IR}[3..0] \\
  100 & \text{SR0} & \text{DR} \leftarrow 0 \& \text{SR}[3..1] \\
  101 & \text{IN} & \text{DR} \leftarrow \text{IN} \\
  110 & \text{OUT} & \text{OUT} \leftarrow \text{DR} \\
  111 & \text{JNZ} & \text{PC} \leftarrow \text{PC} + 1 \text{ if } \text{DR} = 0 \text{ or } \text{PC} \leftarrow \text{IR}[3..0] \text{ if } \text{DR} \neq 0 \text{ (if there is an ADDRESS)} \\
  \end{array} \]

  \( \text{DR}=0 \implies \text{R0 is the destination register}, \text{DR}=1 \implies \text{R1 is the destination register}. \)

  \( \text{SR}=0 \implies \text{R0 is the source register}, \text{SR}=1 \implies \text{R1 is the source register}. \)

- Write an assembly program for a counter from 1 to 5: 1, 2, 3, 4, 5, 1, 2, 3, …. The count must be shown on the output register (OUT).

  start: load R0, 1
          out R0 \rightarrow OUT = 1
          addi R0, 1
          out R0 \rightarrow OUT = 2
          addi R0, 1
          out R0 \rightarrow OUT = 3
          addi R0, 1
          out R0 \rightarrow OUT = 4
          addi R0, 1
          out R0 \rightarrow OUT = 5
          jnz R0, start