Quiz 3
(October 31st @ 9:30 am)

Problem 1 (20 pts)
- Complete the timing diagram of the following state machine:

Problem 2 (25 pts)
- Complete the timing diagram of the circuit whose VHDL description is shown below:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( rs, a, b, x, clk: in std_logic;
         q: out std_logic);
end circ;

architecture hallows of circ is
  signal qt: std_logic;
begin
  process (rs, clk, a, b, x)
  begin
    if rs = '0' then
      qt <= '0';
    elsif (clk'event and clk = '1') then
      if x = '1' then
        qt <= not(qt);
      else
        qt <= a and b;
      end if;
    end if;
  end process;
  q <= qt;
end hallows;
```

Problem 3 (25 pts)
- Sequence detector (with overlap): Draw the state diagram of a circuit that detects the following sequence: 010011. The detector must assert an output ‘z=1’ when the sequence is detected.

Problem 4 (30 pts)
- Complete the timing diagram of the following circuit. \( Q = Q_3 Q_2 Q_1 Q_0 \)