Quiz 2

(October 3rd @ 9:30 am)

PROBLEM 1 (20 PTS)

- Implement the following functions using i) decoders (and gates) and ii) multiplexers:
  - ✓ $F(X,Y,Z) = \overline{X+Y} + Z$
  - ✓ $F(X,Y,Z) = \prod(M_3, M_4, M_7)$

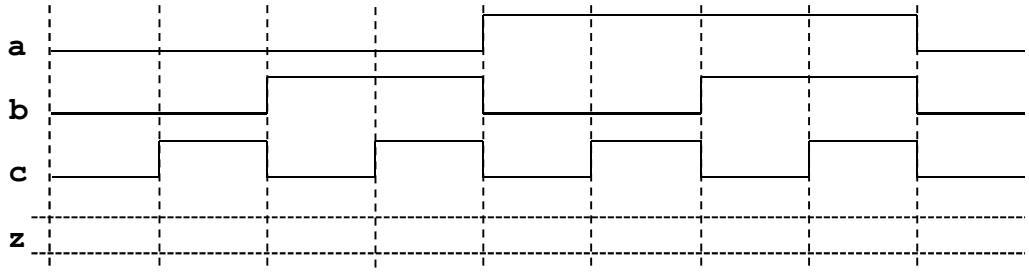
PROBLEM 2 (20 PTS)

- Complete the timing diagram of the circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;

entity tst is
  port (a,b,c: in std_logic;
        z: out std_logic_vector(1 downto 0));
end tst;

architecture bhv of tst is
begin
   process (a,b,c)
   begin
     z <= a & c;
     if b = '1' then
        z <= "01";
     end if;
   end process;
end bhv;
```



PROBLEM 3 (30 PTS)

- Perform the following operations using the 2's complement representation. For each case, provide the summands and the result in 2's complement representation. Use the minimum number of bits to represent the summands and the result so that overflow is avoided.
  - ✓ -17 + 32
  - ✓ -127 - 31

PROBLEM 4 (30 PTS)

- Complete the timing diagram of the circuit shown below: