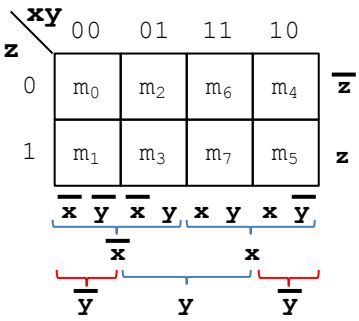
Quiz 1

(September 12th @ 9:30 am)

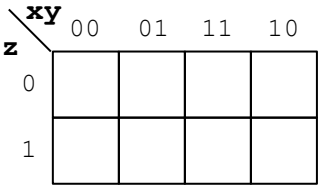
PROBLEM 1 (20 PTS)

Complete the truth table for a circuit that activates an output (f = '1') when the decimal value of the 3 input bits is equal to 1, 4, or 5. Then, simplify the function using Karnaugh maps.

x	y	z	f
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7



x	y	z	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

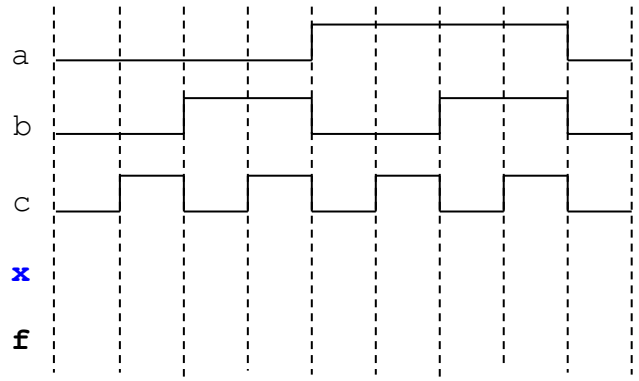


f =

PROBLEM 2 (30 PTS)

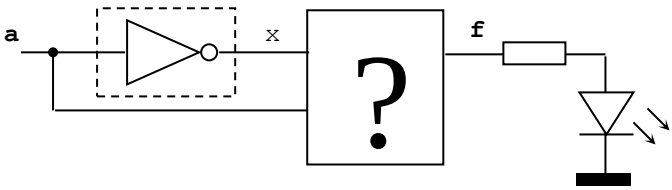
Complete the timing diagram of the logic circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x: std_logic;
begin
  x <= a and b;
  f <= x xnor c;
end st;
```



PROBLEM 3 (20 PTS)

Design a circuit that verifies the logical operation of a NOT gate. f = '1' (LED ON) if the NOT gate works improperly. Assumption: when the NOT gate is not working, it generates 1's instead of 0's and vice versa.



PROBLEM 4 (30 PTS)

a) Convert the following decimal number to i) binary, and ii) hexadecimal. You MUST show your procedure.
   - 113.6875

b) A microprocessor is able to handle memory addresses from 0x0000 to 0x3FFF. How many bits do we need to represent those addresses?