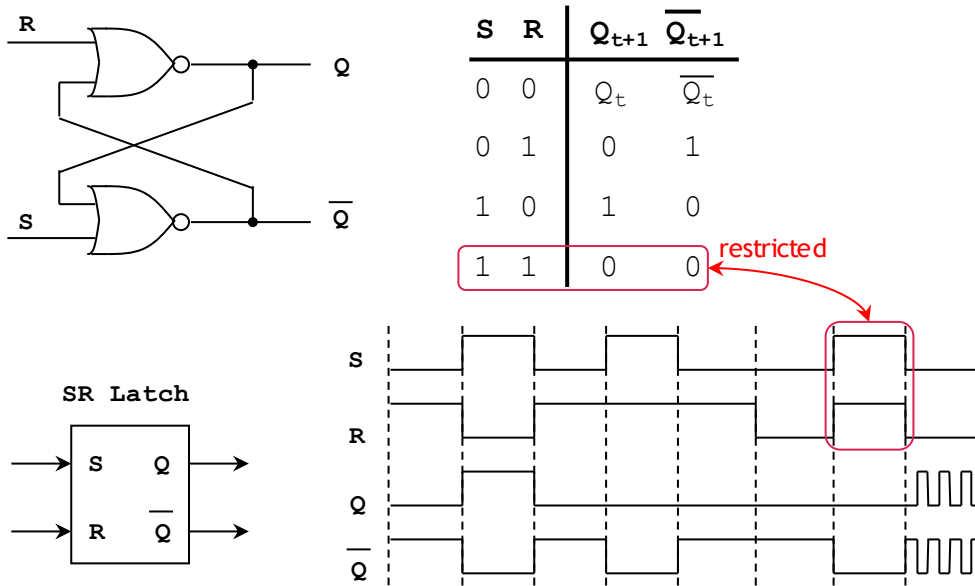


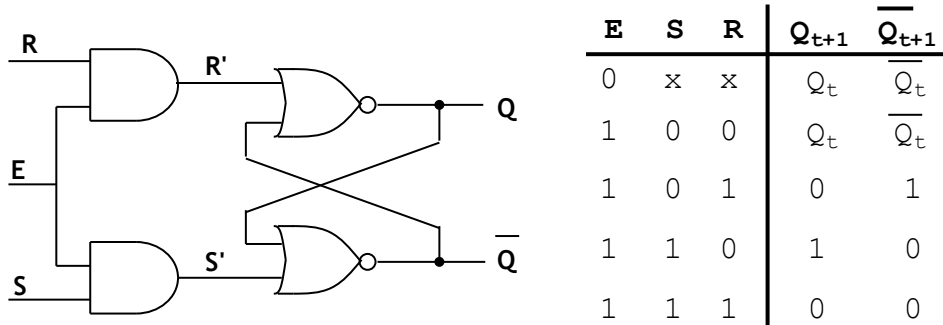
# Notes - Chapter 5

## ASYNCHRONOUS SEQUENTIAL CIRCUITS:

### SR Latch:

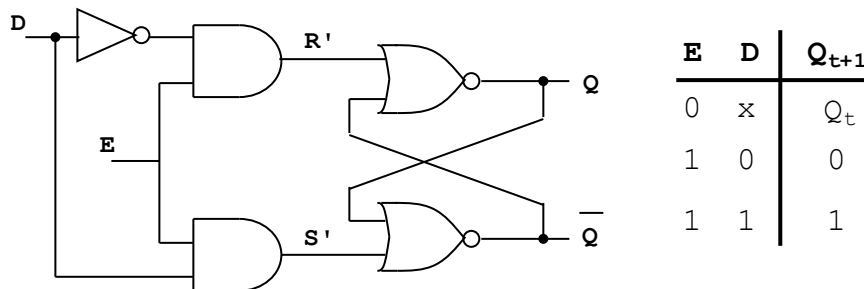


### SR Latch with enable:



### D Latch with enable:

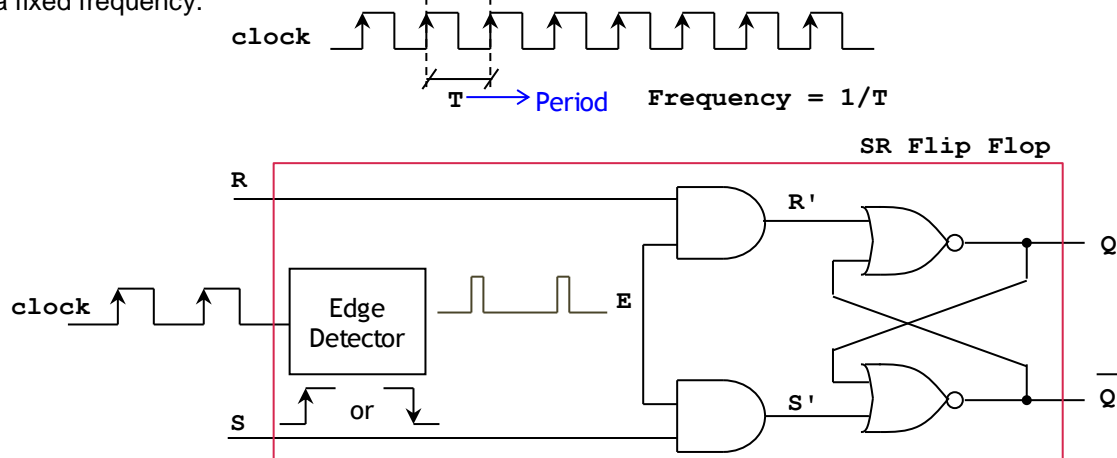
- This is essentially an SR Latch, where  $R = \text{not}(D), S = D$



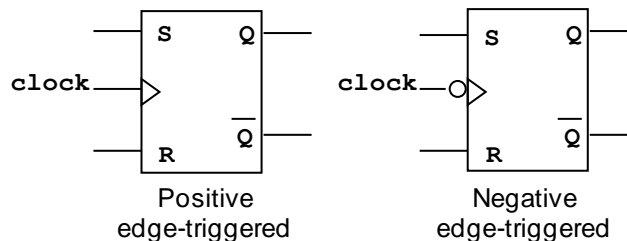
## SYNCHRONOUS SEQUENTIAL CIRCUITS:

### Flip Flops

- Flip flops are made out of:
  - A Latch with an enable input.
  - An Edge detector circuit.
- The figure depicts an SR Latch, where the enable is connected to the output of an *Edge Detector* Circuit. The input to the Edge Detector is a signal called '*clock*'. A clock signal is an square wave with a fixed frequency.

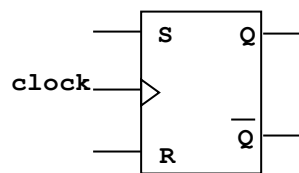


- The edge detector circuit generates short-duration pulses during rising (or falling) edges. These pulses act as enable of the Latch.
- The behavior of the flip flops can be described as that of a Latch that is only enabled during rising (or falling edges).
- Flip flops classification:
  - Positive-edge triggered flip flop: The edge detector circuit generates pulses during rising edges.
  - Negative-edge triggered flip flop: The edge detector circuit generates pulses during falling edges.



### SR Flip Flop

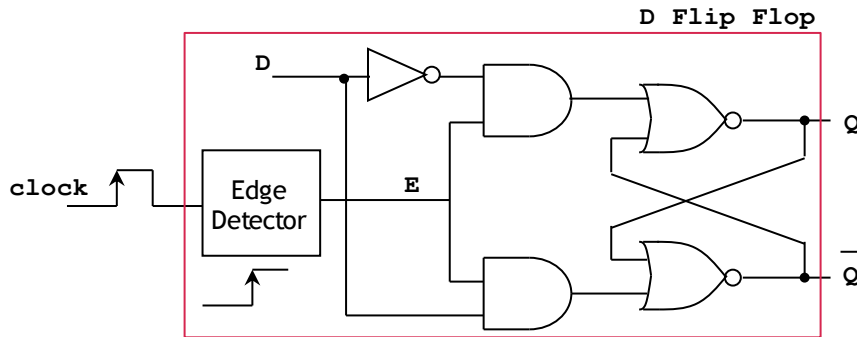
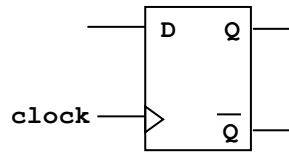
clock	S	R	$Q_{t+1}$	$\overline{Q}_{t+1}$
	0	0	$Q_t$	$\overline{Q}_t$
	0	1	0	1
	1	0	1	0
	1	1	0	0



$$Q_{t+1} = S\overline{R} + Q_t\overline{S}\overline{R} = \overline{R}(S + Q_t\overline{S}) = \overline{R}(S + \overline{S})(S + Q_t) = \overline{R}S + \overline{R}Q_t \text{ (on the edge)}$$

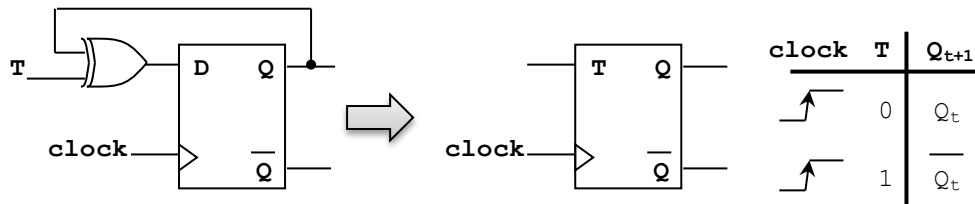
### D Flip Flop

clock	D	$Q_{t+1}$
	0	0
	1	1



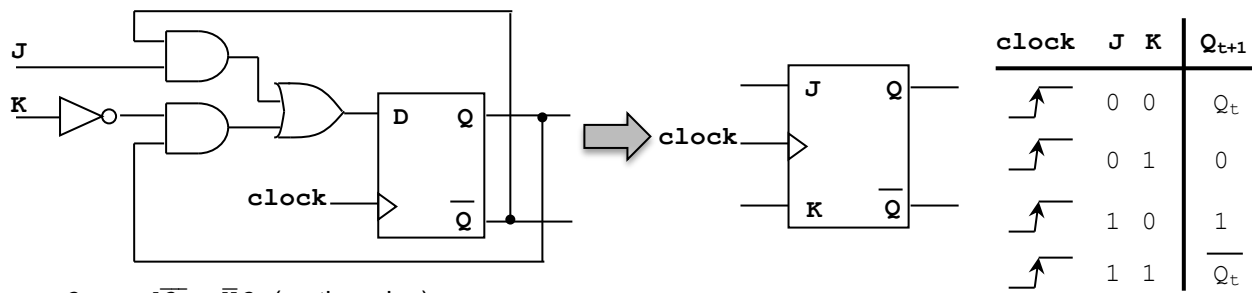
$Q_{t+1} = D$  (on the edge)

### T Flip Flop



$Q_{t+1} = T \oplus Q_t$  (on the edge)

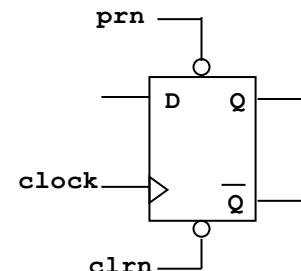
### JK Flip Flop



$Q_{t+1} = J\overline{Q_t} + \overline{K}Q_t$  (on the edge)

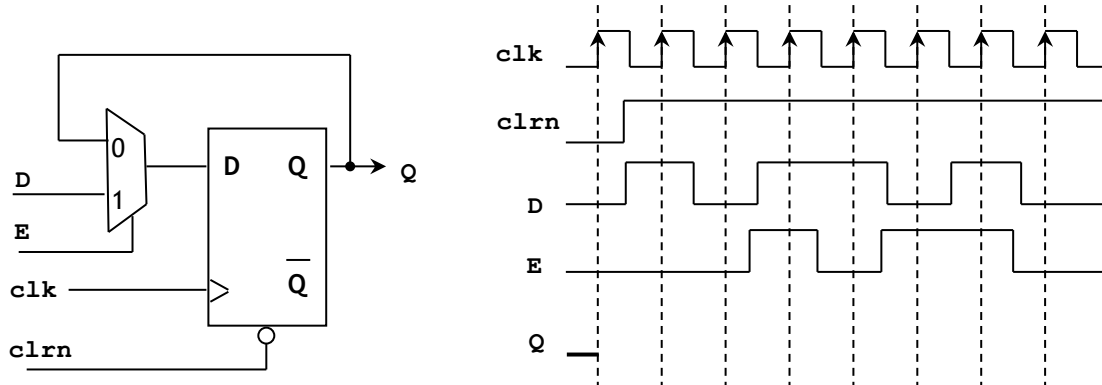
### Synchronous/Asynchronous Inputs

- So far, the flip flops can only change their outputs on the rising (or falling edge). The outputs are usually changed due to a change in the inputs. These inputs are known as *synchronous inputs*, as the inputs' state is only checked on the rising (or falling) edges.
- However, in many instances, it is useful to have inputs that force the outputs to a value immediately, disregarding the rising (or falling edges). These inputs are known as *asynchronous inputs*.
- In the example, we see a D Flip Flop with two asynchronous inputs:
  - `prn`: Preset (active low). When `prn='0'`, the output `q` becomes 1.
  - `clr`: Clear (active low). When `clr='0'`, the output `q` becomes 0.
- If '`prn`' and '`clr`' are both 0, usually `clr` is given priority.
- A Flip flop could have more than one asynchronous inputs, or none.



PRACTICE EXERCISES

1. Complete the timing diagram of the circuit shown below:



2. Complete the VHDL description of the circuit shown below:

```

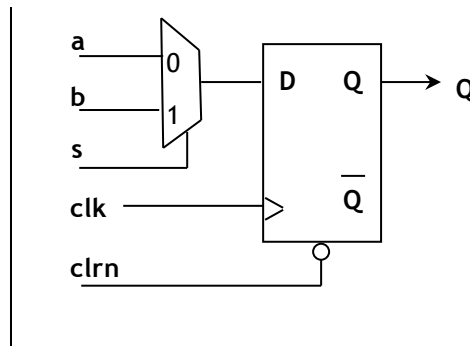
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, s, clk, clr_n: in std_logic;
        q: out std_logic);
end circ;

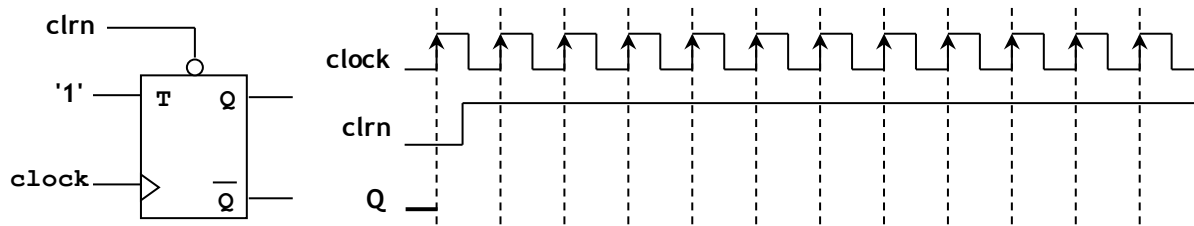
architecture a of circ is

begin
  -- ???
end a;

```



3. Complete the timing diagram of the circuit shown below. If the frequency of the signal clock is 25 MHz, what is the frequency (in MHz) of the signal Q?



4. Complete the timing diagram of the circuit whose VHDL description is shown below:

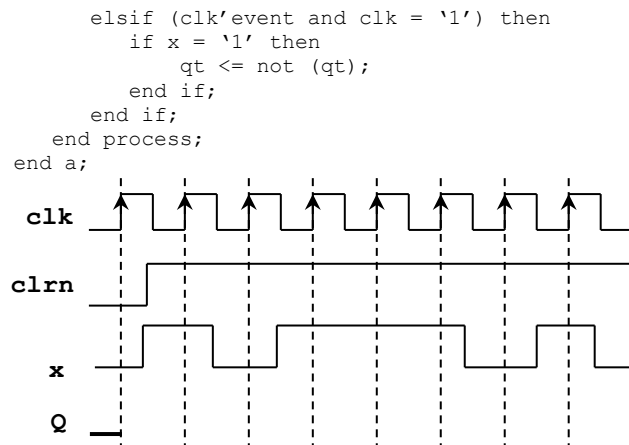
```

library ieee;
use ieee.std_logic_1164.all;

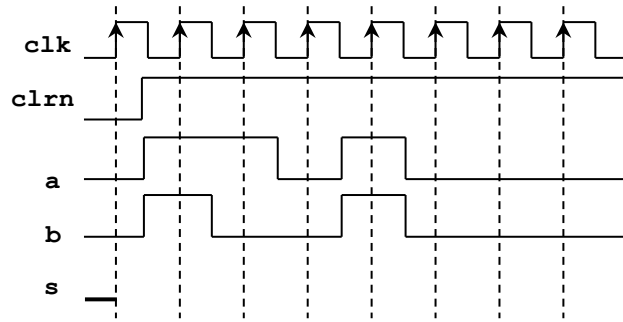
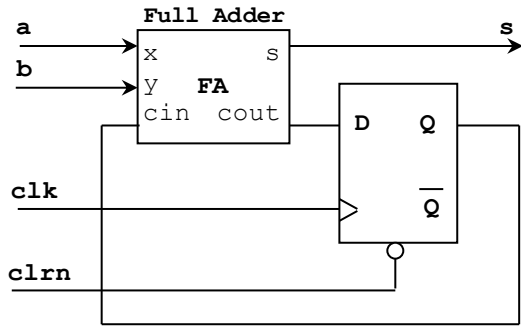
entity circ is
  port ( clr_n, x, clk: in std_logic;
        q: out std_logic);
end circ;

architecture a of circ is
  signal qt: std_logic;
begin
  process (clr_n, clk, x)
  begin
    if clr_n = '0' then
      q <= '0';

```



5. Complete the timing diagram of the circuit shown below:



6. Complete the VHDL description of the synchronous sequential circuit whose truth table is shown below:

```

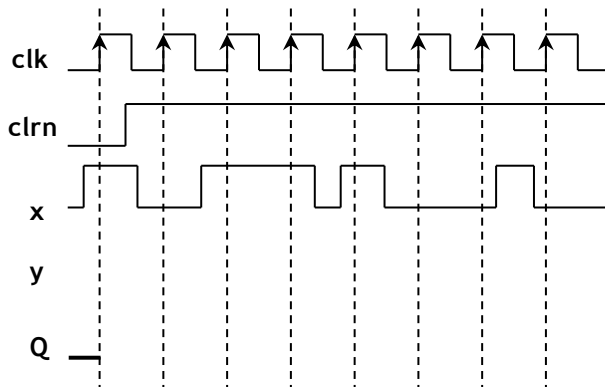
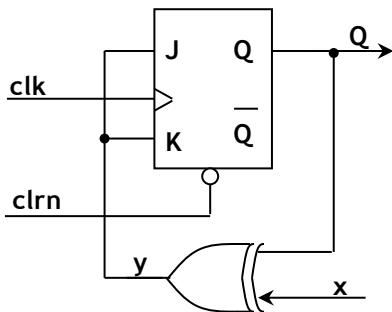
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( A, B, C: in std_logic;
        clrn, clk: in std_logic;
        q: out std_logic);
end circ;

architecture a of circ is
begin
  -- ???
end a;
    
```

clrn	clk	A	B	$Q_{t+1}$
1		0	0	1
1		0	1	C
1		1	0	$Q_t$
1		1	1	$Q_t$
0	X	X	X	0

7. Complete the timing diagram of the circuit shown below:



8. Complete the timing diagram of the circuit shown below:

