Midterm Exam (Online Section)

(Due Date: October 9th @ 11:00 am)
Clarity is very important! Show your procedure!

PROBLEM 1 (15 PTS)

- Complete the following table. Use the fewest number of bits on each case.

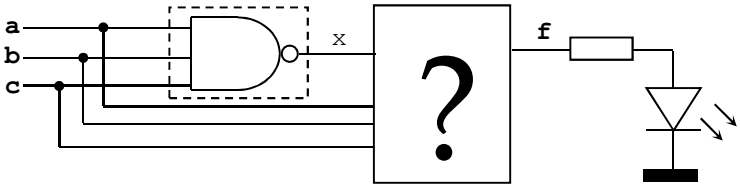
REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
-256			
			101100110
		10010100	
135			

PROBLEM 2 (15 PTS)

a) Convert the decimal number 136.6875 to i) binary, and ii) hexadecimal.
b) Represent the decimal number 136 in i) BCD, and ii) Reflective Gray Code
c) What is the minimum number of bits to represent numbers between 12,000 and 13,024?

PROBLEM 3 (15 PTS)

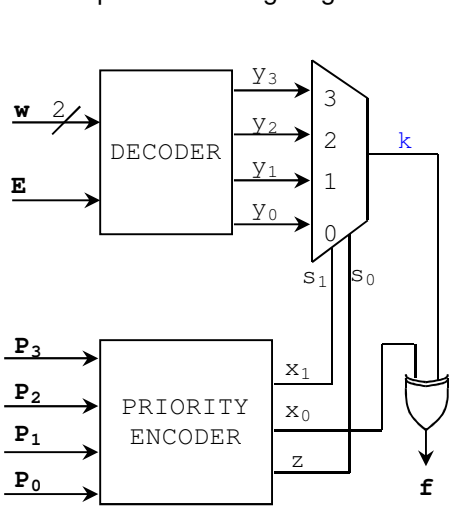
Design a circuit (***simplify your circuit!***) that verifies the logical operation of a 3-input NAND gate. f = '1' (LED ON) if the NAND gate does NOT work properly. Assumption: when the NAND gate is not working, it generates 1's instead of 0's and vice versa.

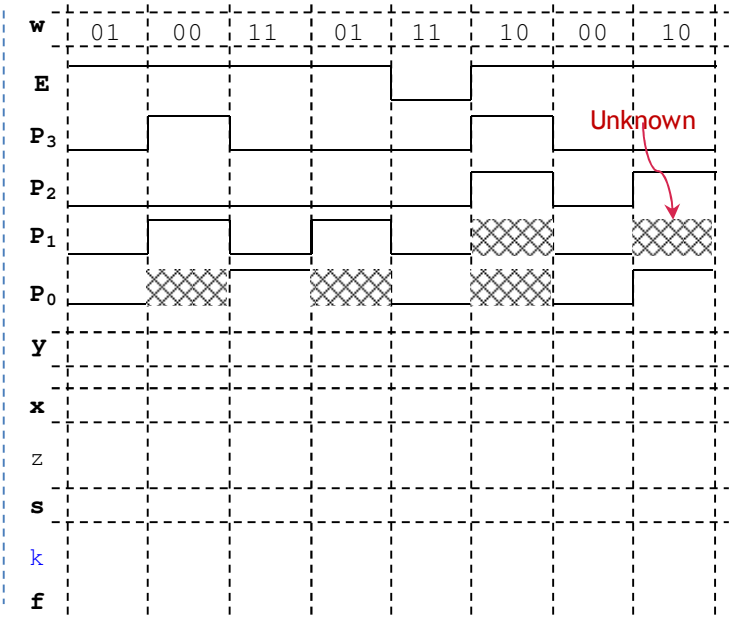


PROBLEM 4 (20 PTS)

- Implement the following function using: i) a decoder (and gates) and ii) a multiplexer:
  - ✓ $F(X,Y,Z) = \prod(M_3, M_4, M_5, M_6)$
  - ✓ $F = X \oplus Y \oplus Z$

- Complete the timing diagram of the circuit shown below:



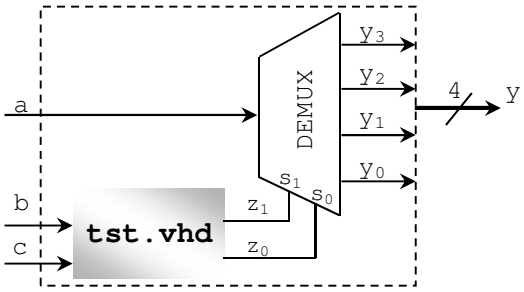


PROBLEM 5 (15 PTS)

- Perform the following operations using the 2's complement arithmetic. For each case, provide the summands and the result in 2's complement representation. Use the minimum number of bits to represent the summands and the result so that overflow is avoided.
  - ✓ `-128 + 453`
  - ✓ `-255 - 37`

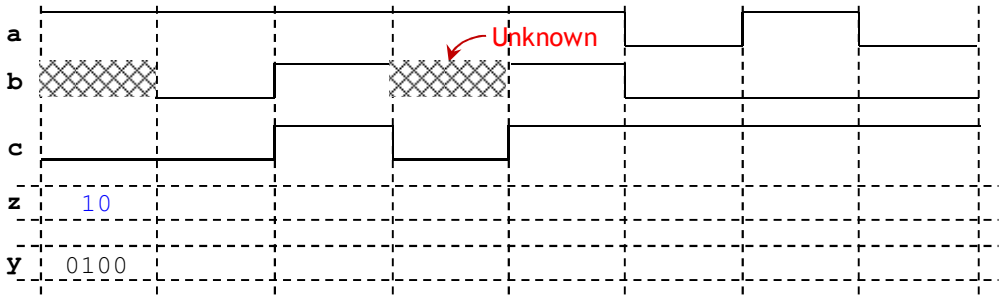
PROBLEM 6 (10 PTS)

- The following VHDL code corresponds to the shaded circuit. Complete the timing diagram:



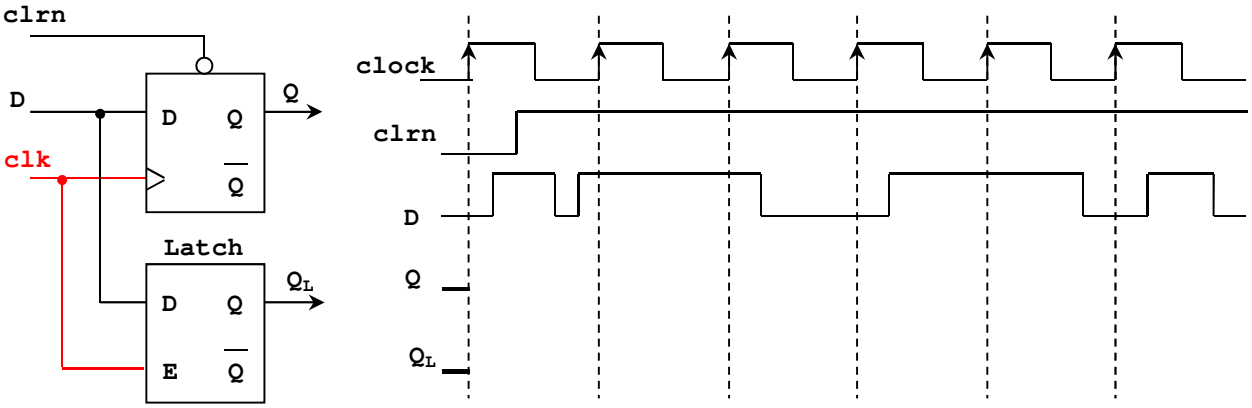

```
library ieee;
use ieee.std_logic_1164.all;

entity tst is
  port (b, c: in std_logic;
        z: out std_logic_vector(1 downto 0));
end tst;
```

```
architecture bhv of tst is
  signal x, y: std_logic;

begin

  process (b,c)
  begin
     z <= c & b;
     if c = '0' then
        z <= "10";
     end if;
  end process;

end bhv;
```



PROBLEM 7 (10 PTS)

- Complete the timing diagram of the circuit shown below:



BONUS PROBLEM (+5 PTS)

- Using ONLY 4-to-1 MUXs, implement an 8-to-1 MUX.
- A microprocessor has a 24-bit address line. We connect a memory chip to the microprocessor. The memory chip addresses are assigned the range `0x800000` to `0xBFFFFF`. What is the minimum number of bits required to represent addresses in that individual memory chip?