Final Exam
(December 10th @ 7:30 am)
Clarity is very important! Show your procedure!

PROBLEM 1 (12 pts)
- Complete the timing diagram of the following circuit. $Q = Q_3Q_2Q_1Q_0$

 PROBLEM 2 (10 pts)
- We want to design a counter modulo-6 (count from 0 to 5) with enable using a State Machine. The counter must assert an output $z=1$ when the count reaches 5.
- Provide the State Diagram (any representation) and the Excitation table $\text{[Inputs][Present State][Next State][Outputs]}$. Is this a Moore or a Mealy machine?

PROBLEM 3 (15 pts)
- Given the following system, complete the Timing Diagram.
- The LUT 6-to-6 implements the following function: $OLUT = \sqrt{ILUT}$
PROBLEM 4 (18 PTS)
- Provide the State Diagram (any representation) of the FSM whose VHDL description is shown below.
- Complete the Timing Diagram.

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( clk, resetn: in std_logic;
         a, b: in std_logic;
         x, w, z: out std_logic);
end circ;

architecture behavioral of circ is
  type state is (S1, S2, S3);
  signal y: state;

begin
  Transitions: process (resetn, clk, a, b)
  begin
    if resetn = '0' then y <= S1;
    elsif (clk'event and clk = '1') then
      case y is
        when S1 =>
          if a = '1' then
            if b = '1' then y <= S2;
            else y <= S1; end if;
          else y <= S1; end if;
        when S2 =>
          if a = '1' then y <= S3;
          else y <= S1; end if;
        when S3 =>
          if b = '1' then y <= S3;
          else y <= S1; end if;
      end case;
    end if;
  end process;

  Outputs: process (y, a, b)
  begin
    x <= '0'; w <= '0'; z <= '0';
    case y is
      when S1 =>
        if a = '1' and b = '1' then z <= '1'; end if;
      when S2 => x <= '1';
      when S3 =>
        if b = '1' then w <= '1'; end if;
    end case;
  end process;
end behavioral;
```

PROBLEM 5 (10 PTS)
- Sequence detector (with overlap): Draw the state diagram (in ASM form) of a circuit (with an input 'x') that detects the following sequence: 10011. The detector must assert and output z='1' when the sequence is detected.
PROBLEM 6 (15 PTS)

- **Basic Processor:**
  - **Available Registers:** R0 (register 0, 4 bits), R1 (register 1, 4 bits), PC (program counter, 4 bits), OUT (output register, 4 bits), IR (instruction register, 8 bits)
  - **Instruction Memory:** Stores up to 16 8-bit instructions.
  - **Instruction Set:** Instructions are specified on the Instruction Register (IR):

  - **OPCODE** (IR[7..5]): Instruction Operation
    - 000: MOV DR, SR
    - 001: LOADI DR, DATA
    - 010: ADD DR, SR
    - 011: ADDI DR, DATA
    - 100: SR0 DR, SR
    - 101: IN DR
    - 110: OUT DR
    - 111: JNZ DR, ADDRESS

  - **DR=0** ⇒ R0 is the destination register, **DR=1** ⇒ R1 is the destination register.
  - **SR=0** ⇒ R0 is the source register, **SR=1** ⇒ R1 is the source register.

  - **IMMEDIATE DATA**

- **Write an assembly program for a counter from 2 to 13:** 2, 3, …, 13, 2, 3, … The count must be shown on the output register (OUT). Use labels to specify any address where your program jumps. Note that you can have only up to 16 instructions.

- **Provide the contents of the Instruction Memory.**
**Problem 7 (20 pts)**

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.